What is claimed is:

1. A bit line pre-charge circuit for a semiconductor memory device, comprising:

first and a second transistors connected in series between a pair of bit lines and each having a gate to which a pre-charge control signal is applied for transimitting a pre-charge voltage to the pair of bit lines in response to the pre-charge control signal; and

a third transistor connected between the pair of bit lines and having a gate receiving the pre-charge control signal as an input for equalizing voltage levels of the pair of bit lines,

wherein the first and second transistors have channel lengths longer than that of the third transistor, so that the first and second transistors have resistances higher than that of the third transistor.

2. A bit line pre-charge circuit of a semiconductor memory device, comprising:

a plurality of pre-charge circuits, each connected between a pair of bit lines for pre-charging the respective pair of bit lines to a pre-charge voltage in response to a pre-charge control signal; and

a pre-charge voltage transmitting circuit for transmitting the pre-charge voltage to the pre-charge circuit in response to the pre-charge control signal,

wherein the pre-charge voltage transmitting circuit is connected to at least two pre-charge circuits.

3. The bit line pre-charge circuit as claimed in claim 2, wherein the pre-charge voltage transmitting circuit has a resistance higher than that of the pre-charge circuits.

4. The bit line pre-charge circuit as claimed in claim 2, wherein the bit-line pre-charge circuit includes:

first and second NMOS transistors connected in series between the pair of bit lines and having a gate receiving the pre-charge control signal as an input for transmitting the pre-charge voltage to the pair of bit lines in response to the pre-charge control signal; and

a third NMOS transistor connected between the pair of bit lines and having a gate receiving the pre-charge control signal as an input for equalizing voltage levels of the pair of bit lines in response to the pre-charge control signal.

5. The bit line pre-charge circuit as claimed in claim 4, wherein the pre-charge voltage transmitting circuit comprises a fourth NMOS transistor connected between a common node of the first and second NMOS transistors and a pre-charge voltage generating line supplying the pre-charge voltage, and having a gate to which the pre-charge control signal is applied.

6. A bit line pre-charge circuit of a semiconductor memory device, comprising:

a plurality of word lines respectively selected in response to a plurality of word line selection signals;

a plurality of pairs of bit lines formed perpendicular to the word lines and selected in response to a plurality of column selection signals;

a plurality of memory cells, each connected between one of the plurality of word lines and one of the plurality of pairs of bit lines; and

a plurality of pre-charge circuits for pre-charging the plurality of pairs of bit lines in response to a plurality of pre-charge control signals,

wherein each of the pre-charge circuits includes first and second NMOS transistors connected in series between a pair of the plurality of pairs of bit lines and having a gate receiving one of the plurality of pre-charge control signals as an input for transmitting a pre-charge voltage to the pair of the plurality of pairs of bit lines in response to the one of the plurality of pre-charge control signals, and a third NMOS transistor connected between the pair of the plurality of pairs of bit lines and having a gate receiving the one of the plurality of pre-charge control signals as an input for equalizing voltage levels of the pair of the plurality of pairs of bit lines in response to the one of the plurality of pre-charge control signals,

and the first and second transistors having channel lengths longer than that of the third transistor, so that the first and second transistors have resistances higher than that of the third transistor.

7. A bit line pre-charge circuit of a semiconductor memory device, comprising:

a plurality of word lines respectively selected by a plurality of word line selection signals;

a plurality of pairs of bit lines formed perpendicular the plurality of word lines and selected by a plurality of column selection signals;

a plurality of memory cells, each connected between a word line of the plurality of word lines and a pair of the plurality of pairs of bit lines;

a plurality of pre-charge circuits for pre-charging the plurality of pairs of bit lines in response to a plurality of pre-charge control signals; and

a plurality of pre-charge voltage transmitting circuits for transmitting a pre-charge voltage to the pre-charge circuits in response to the plurality of pre-charge control signals.

8. The bit line pre-charge circuit as claimed in claim 7, wherein a resistance of each of the pre-charge voltage transmitting circuits is higher than those of the pre-charge circuits.

9. The bit line pre-charge circuit as claimed in claim 7, wherein each of the pre-charge circuits includes:

first and second NMOS transistors connected in series between a pair of the plurality of pairs of bit lines and having a gate receiving a pre-charge control signal of the plurality of pre-charge control signals; and

a third NMOS transistor connected between the pair of the plurality of pairs of bit lines and having a gate receiving the pre-charge control signal.

10. The bit line pre-charge circuit as claimed in claim 9, wherein each of the pre-charge voltage transmitting circuits corresponds to a predetermined number of pre-charge circuits that are adjacent to each other and that are selected by the same column selection signal.

11. The bit line pre-charge circuit as claimed in claim 9, wherein each of the pre-charge voltage transmitting circuits is comprised of a fourth NMOS transistor connected to a common node of the first and second NMOS transistors that form the pre-charge circuits and that are turned on in response to the pre-charge control signal.

12. A bit line pre-charge circuit of a semiconductor memory device that includes a first pre-charge circuit formed in a first bit line area and a second pre-charge circuit formed in a second bit line area, comprising:

a first transistor formed in the first bit line area; and

a second transistor formed in the second bit line area,

wherein a channel of the first transistor starts from a first area of the first bit line area and extends over the second bit line area.

13. The bit line pre-charge circuit as claimed in claim 12, wherein the channel of the first transistor extends to a second area of the first bit line area.

14. The bit line pre-charge circuit as claimed in claim 13, wherein the first and second areas are connected to the same bit line area.

15. The bit line pre-charge circuit as claimed in claim 12, wherein a channel of the second transistor starts from the second bit line area and ends in the first bit line area.

16. A bit line pre-charge circuit of a semiconductor memory device having a first bit line area in which a first transistor is formed and a second bit line area in which a second transistor is formed, comprising:

a first active area in which the first transistor is formed;

a second active area in which the second transistor is formed; and

a third active area in which a third transistor is formed,

wherein one side of the first active area is connected to one side of the second active area and the one side of the second active area is connected to one side of the third active area.

17. The bit line pre-charge circuit as claimed in claim 16, wherein the third transistor is formed across the first bit line area and the second bit line area.

18. The bit line pre-charge circuit as claimed in claim 16, wherein channels of the first, second and third transistors are formed in the first, second and third active areas, respectively.